UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,244	09/29/2003	Christian Muller	59992 (45107)	3489

21874 7590 08/16/2005

EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,244	MULLER ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-23* is/are rejected.

7)☒ Claim(s) *25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 06-15-05. Applicant's arguments with respect to the admitted prior art and reference Ajit et al. (Pub No 2003/0122606A1) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Ajit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14-23 are rejected under 35 U.S.C. 102 (b) being anticipated by Ajit et al. (Pub. No. US 2003/0122606A1).

Regarding claims 14, 15 and 16, figure 18 of Ajit shows a driver circuit comprising: a circuit node (309), two first and second transistors (301, 303 and 305, 307), a control circuit having outputs coupled to the gates of ones of the two first and second transistors (303, 305). When the control circuit is inactive (OE is low), and when the pad voltage is greater than the maximum voltage (Vddo = 3.3V), diode (905) conducts and control voltage (Vgp1) and BIAS-MID increase (col. 6 lines 5-15). The operation of the control circuit depends on the enabling signal (OE) that "changes" or put the driver circuit into an active or inactive state (col. 5 and col. 6). Transistors (303) and (305) function as switches thus, they are in saturation mode when activated (col. 6, [0089]).

Regarding claim 17, figure 11D shows that the electrical path comprises switch controlled by the enabling signal (OE).

Regarding claim 18, element (909b) acts as a resistor.

Regarding claim 19, figures 11D and 18 of Ajit shows a driver circuit comprising: a circuit node (309), two first and second transistors (301, 303 and 305, 307), a control circuit having outputs coupled to ones of the two first and second transistors (303, 305). When the control circuit is inactive (OE is low) and when the pad voltage is greater than the maximum voltage (Vddo = 3.3V), diode (905) conducts and control voltage (Vgp1) and BIAS-MID increase (col. 6 lines 5-15). The operation of the control circuit depends on the enabling signal (OE) that "changes" or put the driver circuit into an active or inactive state (col. 5 and col. 6). The electrical path comprises elements (901), (905), (907), (909b). The transistor (PMOS) of the electrical path in figure 11D is connected to " a further voltage" Vddp and on the other hand with a diode (905). The voltage at the circuit node (PAD) in figure 11D (or the voltage at the circuit node (309) in figure 18 is below voltage Vddp by at least one threshold values (diode 905).

Regarding claims 20-23, figures 11D and 18 of Ajit shows a driver circuit comprising: a circuit node (309), two first and second transistors (301, 303 and 305, 307), a control circuit (901, 905, 907, 909b, 1081, 1101, 1301) regulates the voltages of the gates of the two transistors (303) and (305) dependent on the voltage at the circuit node (309) and the enabling signal (OE). When signal (OE) is high, block (901) generates an output voltage Bias-1 equal to Vddc ([0083]). Figure 11D shows that when signal (OE) is high the output of circuit (901) is clamped to voltage (Vddc). No current flowing through clamping transistor. The rest of circuit (901) does not conduct current when signal (OE) is high. Moreover, when signal (OE) is high, transistor (1081) in figure 18 is turned on to clamp the gate of transistor (303) to a fixed voltage (Vddc), thus no static current flows through transistor (1081). In conclusion, there is no static power consumed when enable signal (OE) is high. All transistors of Ajit's circuit are MOS transistors. The gates of transistors (303) and (305) are controlled by the gate control circuit.

Allowable Subject Matter

Claims 25-27 are objected to because the prior art of records (US 2003/0122606) fails to teach or suggest a driver circuit comprising a switching means controlled by the

enabling signal so that it is conductive in the active state and connects control inputs on one of the two first transistors and one of the two second transistors.

Response to Arguments

In the Remark- pages 7 the Applicant argues that Ajit does not disclose an electrical path having at least one diode; the path is conducting when activated; and device 901 does not include the electrical path which comprises a load section of a transistor controlled by an enable signal.

Figures 11D and 18 of Ajit show an electrical path comprising pad (309), circuit (901) diodes (905) and (909b) and the reference potential (Vddp). When the enable signal (OE) is low, circuit (901) generates an output Bias_Mid. Figure 11D is a detailed circuit of circuit (901). Figure 11D shows a transistor controlled by enabling signal (OE) having load section coupled to diode (905). Diodes (905) and (909b) preset threshold value. Diodes (905) and (909b) belong to the path (pad (309), circuit (901) diodes (905) and (909b) and the reference potential (Vddp).

In page 8, that Applicant argues that Ajit does not disclose the claim 20 recitation of a driver circuit that is configured in such a manner that in the active state it consumes no static power. Column 5, item [0083] discloses that when signal (OE) is high, block (901) generates an output voltage Bias-1 equal to Vddc. Figure 11D that is the circuit of block (901) shows that when signal (OE) is high the two PMOS transistors of the latch leg are turned off. No current flowing through these transistors. The rest of circuit (901) does not conduct current when signal (OE) is high. Moreover, when signal (OE) is high, transistor (1081) in figure 18 is turned on to clamp the gate of transistor (303) to a fixed voltage (Vddc), thus no current flows through transistor (1081). Thus, there is no static power consumed when enable signal (OE) is high.

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
08-08-05

TUAN T. LAM
PRIMARY EXAMINER